APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,754	06/05/2006	Cheng Zheng	42P23020	8501

45209   7590   12/23/2008
INTEL/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER
ROJAS, MIDYS

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
12/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/581,754	ZHENG ET AL.
	Examiner	**Art Unit**	
	MIDYS ROJAS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2008*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date *1/30/2007; 8/08/2006*.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Priority

1.   The examiner acknowledges this application's status as a National Stage

Application under 35 U.S.C. 371 of International Application No. PCT/CN2005/002385,

filed December 30, 2005; from which this application claims priority.

Information Disclosure Statement

2.   The information disclosure statements (IDS) submitted on 8/08/2006 and

1/30/2007 have being considered by the examiner.

Drawings

3.   The drawings filed on 6/5/2006 have been accepted by the examiner.

Specification

4.   The examiner acknowledges that the Abstract of this National Stage Application

under 35 U.S.C. 371 can be found on the front page of the corresponding PCT

publication filed on 8/18/2008. See MPEP § 608.01(b) and MPEP § 1893.03 (e).

Claim Rejections - 35 USC § 112

5.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of
> making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
> set forth the best mode contemplated by the inventor of carrying out his invention.

6.   Claims 12 and 21 rejected under 35 U.S.C. 112, first paragraph, as failing to

comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention. The specification does not provide an appropriate description or definition of the computer-readable medium as claimed.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 9-11 and 18-20 recite the limitation "method device" in lines 1 of each claim. There is insufficient antecedent basis for this limitation in the claim.

9. Claims 14-16 and 22-24 recite the limitation "article device" in lines 1 of each claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

10. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 12 and 21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. These claims are directed towards a computer-readable medium. The specification does not provide a definition for the claimed medium; therefore, the computer readable medium of the claims may any form of medium including non-statutory forms, such a transmission medium or carrier wave. Therefore, Claims 12 and 21 are drawn to non-statutory subject matter.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12.   Claims 1-3, 6-9, 12-14, 17-18, 21-22, and 25-27 are rejected under 35 U.S.C. 103(a) as being obvious over Atri (US 2007/0143532) in view of Sinclair (US 2007/0088904).

Regarding Claim 1, Atri discloses a memory device comprising: an array of memory locations implemented as bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations (bit-alterable non-volatile memory, paragraph 0002); and control circuitry coupled with the array of memory locations (such as that in processors 610 as shown in Figure 6).

Atri does not disclose a control circuitry that causes a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations.

Sinclair discloses a control circuitry that causes a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary). It would have been obvious to one of ordinary skill in the art the time the invention was made to modify the memory of Atri to store data spanning two block of memory by splitting the data with the physical block boundary, as taught by Sinclair, since doing so allows for the efficient use of memory capacity.

Regarding Claim 2, Atri in view of Sinclair discloses the memory device wherein the control circuitry causes a header having an indication of a memory location corresponding to the block of data (additional amount of data storing ECC and overhead related to the user data and the temporary cell group in which it is stored, paragraph 0004) to be stored within the first block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary and wherein a header is stored at the beginning of the block of data and therefore, it must be stored within the first data group when the block is split by the physical block boundary).

Regarding Claim 3, Atri in view of Sinclair discloses the memory device wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material (Atri, paragraph 0019).

Regarding Claim 6, Atri in view of Sinclair discloses the memory device wherein the block of data comprises system data to be used during system initialization and further wherein the block of data is stored in a pre-selected location within the memory array for all initialization sequences (boot code for initialization is stored within ROM 29, paragraph 0038 of Sinclair).

Regarding Claim 7, Atri discloses a method comprising:

receiving data to be stored in a bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations (bit-alterable non-volatile memory, paragraph 0002); and control circuitry coupled with the array of memory locations (such as that in processors 610 as shown in Figure 6).

Atri does not disclose a causing a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations.

Sinclair discloses causing a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary). It would have been obvious to one of ordinary skill in the art the time the invention was made to modify the memory of Atri to store data spanning two block of memory by splitting the data with the physical block boundary, as taught by Sinclair, since doing so allows for the efficient use of memory capacity.

Regarding Claim 8, Atri in view of Sinclair discloses the method further comprising causing a header having an indication of a memory location corresponding to the block of data (additional amount of data storing ECC and overhead related to the user data and the temporary cell group in which it is stored, paragraph 0004) to be stored within the first block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary and wherein a header is stored at the beginning of the block of data and therefore, it must be stored within the first data group when the block is split by the physical block boundary).

Regarding Claim 9, Atri in view of Sinclair discloses the method wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material (Atri, paragraph 0019).

Regarding Claim 12, Atri discloses an article comprising a computer-readable medium having stored thereon instructions that, when executed, cause one or more processors to: receive data to be stored in a bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations (bit-alterable non-volatile memory, paragraph 0002); and control circuitry coupled with the array of memory locations (such as that in processors 610 as shown in Figure 6).

Atri does not disclose a causing a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations.

Sinclair discloses causing a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary). It would have been obvious to one of ordinary skill in the art the time the invention was made to modify the memory of Atri to store data spanning two block of memory by splitting the data with the physical block boundary, as taught by Sinclair, since doing so allows for the efficient use of memory capacity.

Regarding Claim 13, Atri in view of Sinclair discloses the article further comprising instructions that, when executed, cause the one or more processors to

cause a header (additional amount of data storing ECC and overhead related to the user data and the temporary cell group in which it is stored, paragraph 0004) having an indication of a memory location corresponding to the data fragment to be stored within the first block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary and wherein a header is stored at the beginning of the block of data and therefore, it must be stored within the first data group when the block is split by the physical block boundary).

Regarding Claim 14, Atri in view Sinclair discloses the article device wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material (paragraph 0019, Atri).

Regarding Claim 17, Atri discloses a bit-alterable memory (paragraph 0002). Atri does not teach accessing system data during initialization of an electronic system by retrieving data from a pre-selected location, non-volatile memory without scanning multiple memory locations to locate the system data. Sinclair discloses accessing system data during initialization of an electronic system by retrieving data from a pre-selected location (boot data that is to be accessed during initialization from the ROM, paragraph 0038), non-volatile memory without scanning multiple memory locations to locate the system data (wherein accesses to the memory are done without scanning but instead employ the use of conversion tables and maps, paragraph 0036). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Atri to access data without scanning since doing so provides for faster access times.

Regarding Claim 18, Atri in view of Sinclair discloses the method wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material (Atri paragraph 0019).

Regarding Claim 21, Atri discloses a bit-alterable memory (paragraph 0002). Atri does not teach an article comprising a computer-readable medium having stored thereon instructions that, when executed, cause one or more processors to access system data during initialization of an electronic system by retrieving data from a pre-selected location in a bit-alterable, non-volatile memory without scanning multiple memory locations to locate the system data. Sinclair discloses accessing system data during initialization of an electronic system by retrieving data from a pre-selected location (boot data that is to be accessed during initialization from the ROM, paragraph 0038), non-volatile memory without scanning multiple memory locations to locate the system data (wherein accesses to the memory are done without scanning but instead employ the use of conversion tables and maps, paragraph 0036). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Atri to access data without scanning since doing so provides for faster access times.

Regarding Claim 22, Atri in view of Sinclair discloses the article device wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material (Atri paragraph 0019).

Regarding Claim 25, Atri discloses a system comprising:

an antenna (Fig. 6, 685);

a memory system coupled with the antenna, the memory system having an array of memory locations implemented as bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations (bit-alterable non-volatile memory, paragraph 0002); and control circuitry coupled with the array of memory locations (such as that in processors 610 as shown in Figure 6).

Atri does not disclose a control circuitry that causes a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations.

Sinclair discloses a control circuitry that causes a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block boundary). It would have been obvious to one of ordinary skill in the art the time the invention was made to modify the memory of Atri to store data spanning two block of memory by splitting the data with the physical block boundary, as taught by Sinclair, since doing so allows for the efficient use of memory capacity.

Regarding Claim 26, Atri in view of Sinclair discloses the system wherein the control circuitry causes a header having an indication of a memory location corresponding to the block of data (additional amount of data storing ECC and overhead related to the user data and the temporary cell group in which it is stored, paragraph 0004) to be stored within the first block of memory locations (paragraph 0009 wherein a transformed data unit may be split into two or more data groups by a physical block

boundary and wherein a header is stored at the beginning of the block of data and therefore, it must be stored within the first data group when the block is split by the physical block boundary).

Regarding Claim 27, Atri in view of Sinclair discloses the system wherein the bit-alterable, non-volatile memory includes cells including a thin film chalcogenide alloy material (Atri paragraph 0019).

13.   Claims 4-5, 10-11, 15-16, 19-20, 23-24, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atri (2007/0143531) in view of Sinclair (2007/0088904) as applied to claims 1-3, 6-9, 12-14, 17-18, 21-22, and 25-27, above, and further in view of Zaidi (2006/0245236).

Regarding Claims 4, 10, 15, 19, 23, and 28, Atri in view of Sinclair discloses the invention of claims 3, 9, 14, 18, 22, and 27 above. Atri in view of Sinclair does not teach the chalcogenide alloy material comprises GeSbTe. Zaidi discloses a chalcogenide alloy material comprising GeSbTe (paragraph 0058). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Atri in view of Sinclair to include a chalcogenide alloy material comprising GeSbTe since this is a well known composition for chalcogenide alloy materials.

Regarding Claims 5, 11, 16, 20, 24, and 29, Atri in view of Sinclair discloses the invention of claims 3, 9, 14, 18, 22, and 27 above. Atri in view of Sinclair does not teach the chalcogenide alloy material is selected from the group consisting of: GaSb, InSb, InSe, Sb_2Te_3, GeTe, $Ge_2Sb_2Te_5$, InSbTe, GaSeTe,

SnSb.sub.2Te.sub.4,   InSbGe,   **AgInSbTe**,   (GeSn)SbTe,   GeSb(SeTe),   and

Te.sub.81Ge.sub.15Sb.sub.2S.sub.2.   Zaidi discloses a chalcogenide alloy material

comprising AgInSbTe (paragraph 0058). It would have been obvious to one of ordinary

skill in the art at the time the invention was made to modify the invention of Atri in view

of Sinclair to include a chalcogenide alloy material comprising AgInSbTe since this is a

well known composition for chalcogenide alloy materials.

The applied reference (Atri 2007/0143531) has a common assignee with the

instant application. Based upon the earlier effective U.S. filing date of the reference, it

constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a)

might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed

but not claimed in the reference was derived from the inventor of this application and is

thus not an invention "by another"; (2) a showing of a date of invention for the claimed

subject matter of the application which corresponds to subject matter disclosed but not

claimed in the reference, prior to the effective U.S. filing date of the reference under 37

CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application

and reference are currently owned by the same party and that the inventor named in the

application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer

in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing

that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under

35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MIDYS ROJAS whose telephone number is (571)272-4207. The examiner can normally be reached on M-TH 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Midys Rojas/
Examiner, Art Unit 2185

MR